Japanese Patent 10-242078

Multi-layer electrode using conductive oxide

By Sharp Corporation, Osaka, Japan

Summary

Subject:

To provide a multi layer electrode that has properties as following:

1. electrode itself has no hillocks or peelings;
2. no oxygen diffusion to poly silicon underneath;
3. electrode is dense and has smooth surface;
4. remaining low resistance after high temperature process above 600C in oxygen ambient.

Approach:

The multi layer electrode on a semiconductor substrate will have a barrier layer on its lower part, which can be either TaSiN or HfSiN; and a conductive oxide of IrO2/Ir above the barrier layer.

Claims:

1. The multi layer electrode on a semiconductor substrate, of which the unique is that there is a barrier layer on its lower part consisting of Ta or Hf and Si, N; and a conductive oxide of IrO2/Ir above the barrier layer.
2. In the multi layer electrode of claim 1, IrO2 and Ir are crystalline thin film with the <100> and <111> orientation for IrO2 and Ir respectively;
3. Film thickness of IrO2/Ir multi layer electrode of either claim 1 and claim 2 is less than 150nm;
4. Multi layer electrode of claim 1 ~ 3 which has Ir thick enough to prevent the oxidation of the barrier layer;
5. The thickness of Ir layer of claim 4 is larger than 22nm;
6. Multi layer electrode of claim 1 ~ 5 which has IrO2 thick enough to prevent the oxidation of the barrier layer during the high temperature annealing;
7. The thickness of IrO2 layer of claim 6 is larger than 36nm;

Detail description

Field of the invention:

The invention is related to the multi layer electrode using conductive oxide more specifically, related to the multi layer electrode used as the bottom electrode in the various devices with ferroelectric thin film oxides such as ferroelectric nonvolatile memories, DRAM and infrared sensors.

Previous arts and problems: Omitted

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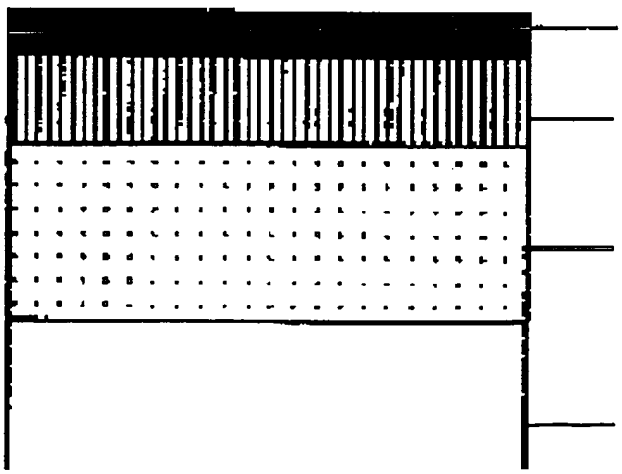
(54) MULTILAYER ELECTRODE USING OXIDE CONDUCTOR

(57) Abstract:

PROBLEM TO BE SOLVED: To avoid forming hillocks or peeling an electrode and block O from diffusing in lower polysilicon plugs, by forming an IrO2/Ir laminate structure electrode on a barrier metal contg. Ta, Hf and Si and N as component elements.

SOLUTION: On a single crystal Si (100) wafer 1 an SiO2 film 2 of 600nm thick, Ta5SiN4 barrier metal 3 of 100mm and IrO2 (230nm), Ir (130nm) or IrO2 (82nm)/Ir (66nm) electrode layer 4 are laminated to form a multilayer electrode which has a durability enough to a heat process in an O-atmosphere over 600°C. For the IrO2 or Ir a crystal film oriented



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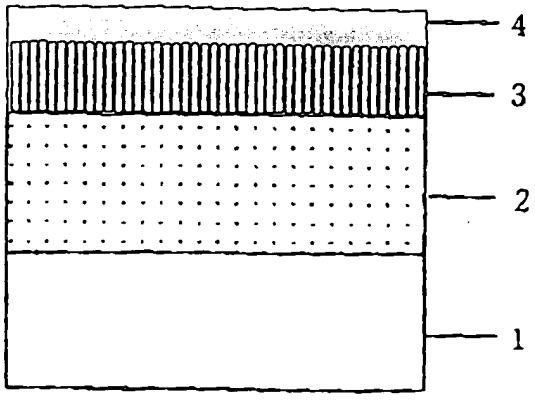
(54)【発明の名称】　酸化物導電体を用いた多層構造電極

(57)【要約】

【課題】　①電極自体にヒロックや剥離が発生せず、②下部ポリシリコンプラグへの酸素拡散がなく、③電極の表面平坦性、緻密性が確保され、④電極としてシート抵抗等の電気特性が確保される、６００℃以上の酸素雰囲気中での熱処理工程に対するプロセス耐性を有する電極を実現できる多層構造電極を提供することを目的とする。

【解決手段】　半導体基板上に形成される多層構造電極において、下部にＴａＳｉＮ、ＨｆＳｉＮのいずれか一つから選択されたバリアメタルを有し、該バリアメタルの上部にＩｒO_2／Ｉｒ積層構造電極が形成されてなる酸化物導電体を用いた多層構造電極。



とは言えない。例えば、ゾルーゲル法によりＰＺＴ膜を上記のＰｔ／ＴｉＮ／Ｔｉ電極上に形成する際、４００～４５０℃の仮焼成段階ではヒロック発生や剥離は発生しないが、６００℃以上の本焼成でこれらの問題が発生することが知られているからである。

【０００８】本発明は上記課題に鑑みなされたものであり、ＳＴＣ構造に適用可能なプロセス耐性に優れた電極の開発の必要から、①電極自体にヒロックや剥離が発生せず、②下部ポリシリコンプラグへの酸素拡散がなく、③電極の表面平坦性、緻密性が確保され、④電極としてシート抵抗等の電気特性が確保される、６００℃以上の酸素雰囲気中での熱処理工程に対するプロセス耐性を有する電極を実現できる多層構造電極を提供することを目的とする。

【０００９】

【課題を解決するための手段】本発明によれば、半導体基板上に形成される多層構造電極において、下部にＴａ又はＨｆ、およびＳｉ、Ｎを構成元素とするバリアメタル（以下、「ＴａＳｉＮ又はＨｆＳｉＮ」と記す）を有し、該バリアメタルの上部にIrO_2／Ｉｒ積層構造電極が形成されてなる酸化物導電体を用いた多層構造電極が提供される。

【００１０】

【発明の実施の形態】本発明における多層構造電極は、強誘電体不揮発性メモリ、ＤＲＡＭ、赤外線センサアレイ等における強誘電体薄膜の下部電極として用いることができるものであり、半導体基板上に形成される。半導体基板としては、通常上記素子の基板として用いることができるものであれば、特に限定されるものではなく、例えばシリコン基板、ＧａＡｓ、ＩｎＧａＡｓ等の化合物半導体基板等を使用することができる。本発明の多層構造電極は、半導体基板上に直接形成してもよいし、ＳｉＮ、SiO_2 等の絶縁膜を介して形成してもよいし、キャパシタ、トランジスタ又は金属配線等の所望の素子を形成した上に層間絶縁膜を介して形成してもよい。例えば、絶縁膜を介して形成する場合には、絶縁膜の膜厚は５００～２０００ｎｍ程度が好ましく、所望の素子及び層間絶縁膜を介して形成する場合には、層間絶縁膜は、素子と電極との絶縁性を確保することができる十分な膜厚であることが好ましい。これら絶縁膜等は、公知の方法、例えばＣＶＤ法、スピンコート法等により形成することができる。この際の成膜温度は、６００℃程度以下であることが好ましい。

【００１１】本発明の多層構造電極は、バリアメタルとしてＴａＳｉＮ又はＨｆＳｉＮのいずれかを用いた電極であり、具体的には、IrO_2／Ｉｒ／ＴａＳｉＮ又はIrO_2／Ｉｒ／ＨｆＳｉＮの多層構造電極である。バリアメタルであるＴａＳｉＮ又はＨｆＳｉＮ膜は、例えば１００～５００ｎｍ程度の膜厚で、公知の方法、例えばＲＦマグネトロンスパッタ法、ＤＣマグネトロンスパッタ法、真空蒸着法、電子ビーム蒸着法等種々の方法で形成することができる。ここで、ＴａＳｉＮ又はＨｆＳｉＮ膜をバリアメタルとして用いるには、一般にアモルファス構造が望ましいため、その組成比は自由に変更することができる。

【００１２】また、バリアメタル直上に形成される積層構造電極を構成するＩｒ膜は、公知の方法、例えば、ＲＦマグネトロンスパッタ法、ＤＣマグネトロンスパッタ法、真空蒸着法、電子ビーム蒸着法等種々の方法で、後の工程におけるIrO_2 層の形成に際して、下部のバリアメタルの酸化を抑止するのに十分な膜厚で形成することが好ましい。この膜厚は、例えば、２２ｎｍ以上があげられる。また、Ｉｒ層は（１１１）面に配向して形成されることが好ましい。具体的には、ＲＦマグネトロンスパッタ法の場合は、ＲＦパワー８０～２００Ｗ程度、基板温度を２００～２７０℃程度に保持しながら、スパッタガスとしてＡｒ、Ｎ等の不活性ガスを用いて成膜する方法があげられる。

【００１３】また、Ｉｒ膜上に形成されるIrO_2 膜は、公知の方法、例えば、上述と同様の方法で、後述する積層構造電極の高温アニールに際して下部のバリアメタルの酸化を抑止するに十分な膜厚で形成することが好ましい。この膜厚は、例えば、３６ｎｍ以上があげられる。但し、IrO_2 ／Ｉｒ膜の総膜厚が１５０ｎｍ以下、さらに６０ｎｍ以上で形成されることが好ましい。また、IrO_2 層は（１００）面に配向して形成されることが好ましい。具体的には、ＲＦマグネトロンスパッタ法の場合は、ＲＦパワー８０～２００Ｗ程度、基板温度を２００～２７０℃程度に保持しながら、スパッタガスとしてＡｒ、Ｎ等の不活性ガスに酸素ガスを１：１０～１０：１程度の割合で混合したガスを用いて成膜する方法があげられる。

【００１４】このような多層積層電極により、６００℃以上の酸素雰囲気中での熱処理プロセスに十分な耐性を有する電極構造を実現できる。また、IrO_2では（１００）面、Ｉｒでは（１１１）面に配向した結晶薄膜を用いることにより、微結晶粒からなる緻密な表面平坦性に優れた積層電極構造を実現することができる。このような表面平坦性、緻密性を備えた配向性の多層積層電極は、強誘電体薄膜の下地電極として適するだけでなく、電極自体のシート抵抗までも制御できることとなり、種々の素子の電極として使用することができる。以下に、本発明の酸化物導電体を用いた多層構造電極について説明する。

【００１５】実施例１

本発明の多層構造電極は、図１に示したように、単結晶Ｓｉ（１００）ウエハ１の表面に６００ｎｍの厚さのSiO_2 膜２、その上にバリアメタル３としてＴａＳｉＮ（１００ｎｍ）、さらにその上に電極層４としてIrO_2（２３０ｎｍ）、Ｉｒ（１３０ｎｍ）、IrO_2（８２

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きれていない、あるいはその後のIrO_2形成時の酸素プラズマによる酸化を抑止できない程度に膜厚が薄いためにTaSiNが酸化される箇所が存在し、そこでのストレスがヒロックを発生させたと考えられる。

【0026】その他のサンプルについては全てアニール後においても剥離、ヒロック等は見られず、アニール耐性のあることが確認できた。作製したサンプルの中で最も膜厚の薄いIrO_2（36nm）／Ir（22nm）／TaSiN構造のアニール後の断面をSEM観察したところ、IrO_2／Irの膜厚が60nm程度と薄い場合においても平坦性が保たれており、TaSiN部分も反応や拡散等は見られなかった。

【0027】すなわち、（100）に配向したIrO_2及び（111）配向したIrからなるIrO_2／Ir積層電極構造を用いることで、非常に緻密で60nm程度の薄い導膜で酸化物強誘電体導膜の成膜プロセス耐性を実現できた。更に、作製したサンプルについてシート抵抗を測定したところ、図3に示すようにIrO_2／Ir積層電極におけるIr層及びIrO_2層の膜厚を変えることで電極全体のシート抵抗を1．2～2．8Ω／□の範囲で制御できることが分かった。

【0028】また、バリアメタルとしてHfSiNを用いたIrO_2／Ir／HfSiN構造においても、少なくともIrO_2／Ir電極の膜厚が約60nm～150nmの範囲で同様に剥離、ヒロックのない平坦で緻密な電極構造を作製でき、かつ酸素中での高温アニール耐性が得られることを確認できた。以上で述べたように、本発明のIrO_2／Ir電極構造を用いることで平坦性、緻密性に優れた電極を作製できる。その結果、Ir層の膜厚が22nm以上でかつIrO_2層の膜厚が36nm以上の条件においてIrO_2／Ir電極の膜厚が約60～150nmと薄いプロセス耐性に優れた電極が作製できた。さらに、シート抵抗が各層の膜厚を変えることにより1．1～2．8Ω／□まで制御できた。

【0029】

【発明の効果】本発明によれば、STC構造を用いた強誘電体メモリやDRAMの実用化に不可欠なプロセス耐性に優れた下部電極が再現性良く作成することができる。特に、IrO_2層及びIr層が結晶薄膜であり、IrO_2層は（100）面に配向し、Ir層は（111）面に配向してなる場合には、その電極は平坦性、緻密性にも優れるため、微細加工プロセス等への適用性も高くなる。

【0030】さらに、IrO_2／Ir層の膜厚が150nm以下である場合には、積層構造電極の各層の膜厚を変えることでシート抵抗等の電気特性の制御も可能となる。このように、本発明の多層構造電極においては、例えば、強誘電体膜の形成プロセスにおいて、下部の半導体との反応、相互拡散を防止することができ、信頼性の高い、良好な特性を有する素子を得ることが可能となる。

【図面の簡単な説明】

【図1】本発明の酸化物導電体を用いた多層構造電極の実施例を示す概略断面図である。

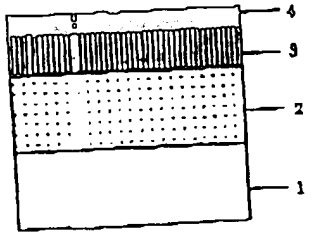
【図2】本発明の多層構造電極のIrO_2／Ir／TaSiN構造のアニール後の表面及び断面のSEM写真である。

【図3】本発明の多層構造電極のIrO_2／Ir／TaSiN構造のシート抵抗を示すグラフである。

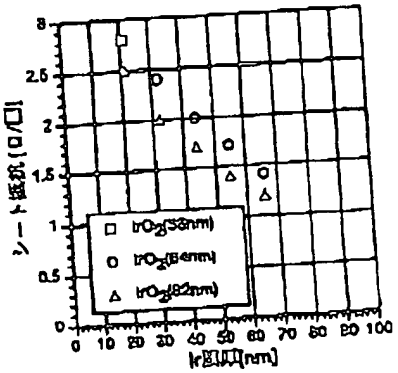
【符号の説明】

1　単結晶Si基板
2　SiO_2膜
3　バリアメタル
4　電極層

【図1】



【図3】



DETAILED DESCRIPTION

[Detailed description]
[0001]
[The technical field to which invention belongs] this invention relates to the multilayer-structure electrode used as a lower electrode of a ferroelectric thin film in the various devices which applied the oxide ferroelectric to the detail more, for example, ferroelectric non-volatile memory, DRAM, an infrared sensor array, etc. about the multilayer-structure electrode which used the oxide conductor.
[0002]
[A Prior art and Object of the Invention] In recent years, the development of ferroelectric memory is performed as non-volatile memory which has the high integration about the same as DRAM, a fast turn around, a low power, and high-reliability. As a memory capacitor material for ferroelectric memory, the crystal thin film of the oxide ferroelectrics including PZT (titanic-acid lead zirconate), SrBi2Ta2O9, and Bi4Ti3O12 is used.
[0003] When forming the crystal thin film of an oxide ferroelectric, 600-800-degree C elevated-temperature heat treatment is usually needed in the ambient atmosphere containing oxygen. Therefore, many Pts the lower electrode formed caudad excelled Pts] in oxidation resistance with the high-melting point have been used. On the other hand, implementation of stack cell (STC) structure is desired for high integration of a memory device. It is necessary to connect a semiconductor transistor and a ferroelectric memory capacitor with plugs, such as contest polysilicon, in STC structure. However, although the conventional Pt electrode is excellent in oxidation resistance, it has the trouble of being easy to penetrate oxygen. For this reason, when Pt electrode is formed on a polysilicon contest, in case a ferroelectric thin film is formed, contest polysilicon used for the plug will oxidize, and the problem that electric connection is not obtained arises.
[0004] On the other hand, multilayer-structure electrodes, such as Pt/TiN/Ti which used Ti as a glue line between TiN, a plug, and a lower electrode, are examined as a barrier layer for preventing oxygen transparency. However, TiN layer oxidizes by the oxygen which penetrated Pt also in this case, and the new problem of the sublation by the Pt/TiN interface or hillock occurrence has arisen for the cubical expansion (43rd 1996 spring collection of applied physics relation union lecture meeting lecture drafts 28p-V- 6, 7).
[0005] moreover, using an oxide conductor material also inquires as a lower electrode -- having -- **** -- among these, IrO2, RuO2, and YBa2Cu3O7- promising ** of X, LaSrCoO3, etc. is carried out from points, such as the outstanding barrier nature and the adjustment with an oxide ferroelectric The example by which especially IrO2 was directly formed on the polysilicon contest is reported. For example, it is indicated by the Japanese Patent Publication No. 87493 [six to] official report that produce BaTiO3 and a good dielectric characteristics is obtained on IrO2 / polysilicon contest. moreover, in Appl.Phys.Lett.vol.65(1994) pp.1522-1524, Jpn.J.Appl.Phys.vol.33(1994) pp.5207-5210, and a publication-number 51165 [eight to] official report When PZT is formed on contest polysilicon [Ir/IrO2 /], or Pt/IrO2 / polysilicon contest, It is mentioned that it is indicated that the lassitude property is improved sharply and IrO2 layer has good barrier nature to ferroelectric configuration elements, such as Pb, as this ground.
[0006] However, we are anxious about the occurrence with a poor contact by oxidization of a polysilicon contest front face when forming IrO2 of a direct oxide on a polysilicon contest like such structures. Then, the study of the multilayer electrode of IrO2/Ir/TiN / Ti structure which inserted barrier metal between contest polysilicon and IrO2 is reported (collection of 43rd 1996 spring applied physics relation union lecture meeting lecture drafts 28p- V-4). According to this report, the high dielectric SrTiO3 (200nm) is formed on the electrode which carried out structure of IrO2 (100nm) / Ir(50nm)/TiN (30nm) / Ti (20nm) / Si substrate formed by the spatter. In the capacitor which used Pt (50nm) as the up electrode, 216 or less specific inductive capacity and the two or less cm [leakage-current density 10-7A/cm] comparatively good electrical property have been acquired, and it is shown that this multilayer-structure electrode is promising for an application of STC structure, and it is.
[0007] However, about the oxygen barrier nature of this multilayer-structure electrode, and reaction tightness, it is unknown. That is, SrTiO3 cannot say obvious whether there is enough of the process resistance, when this multilayer-structure electrode is applied to the **** process of a ferroelectric thin film which needs the **** temperature of 600 degrees C or more, although usually formed at the comparatively low temperature of 500 degrees C or less. For example, it is because it is known for the 400-450-degree C temporary baking phase that these problems will occur by this baking of 600 degrees C or more although neither hillock occurrence nor sublation is generated in case PZT layer is formed on the above-mentioned Pt/TiN / Ti electrode by the ********** method.

[0008] From the need for a development of an electrode of this invention being made in view of the above-mentioned technical probrem, and having excelled in process resistance applicable to STC structure ** Neither a hillock nor sublation occurs in the electrode itself, but there is no oxygen diffusion to ** lower polysilicon contest plug. ** Aim at offering the multilayer-structure electrode which can realize the electrode which has the process resistance over the heat treatment process in the inside of the oxygen ambient atmosphere 600 degrees C or more that the surface flat nature of an electrode and compactness are secured and electrical properties, such as sheet resistance, are secured as a ** electrode.
[0009]
[The means for solving a technical problem] According to this invention, in the multilayer-structure electrode formed on a semiconductor substrate, it has the barrier metal (it is hereafter described as "TaSiN or HfSiN") which uses Ta or Hf, and Si and N as a configuration element at the lower part, and the multilayer-structure electrode using the oxide conductor which comes to form IrO2 / Ir laminated-structure electrode in the upper part of this barrier metal is offered.
[0010]
[Gestalt of implementation of invention] The multilayer-structure electrode in this invention can be used as a lower electrode of a ferroelectric thin film in ferroelectric non-volatile memory, DRAM, an infrared sensor array, etc., and is formed on a semiconductor substrate. As a semiconductor substrate, if it can usually use as a substrate of the above-mentioned element, especially, it is not limited and compound semiconductor substrates, such as a silicon substrate, and GaAs, InGaAs, etc. can be used. You may form directly on a semiconductor substrate and the multilayer-structure electrode of this invention is SiN and SiO2. You could form through the insulator layer of a grade, the element of requests, such as a capacitor, a transistor, or a metal wiring, was formed upwards, and you may form through a layer insulation layer. For example, when forming through an insulator layer, the thickness of an insulator layer has desirable about 500-2000nm, and when forming through a desired element and a desired layer insulation layer, it is desirable [a layer insulation layer] that it is sufficient thickness which can secure the insulation of an element and an electrode. These insulator layers etc. can be formed by well-known technique, for example, CVD, the spin coat method, etc. As for the **** temperature in this case, it is desirable that it is about 600 degrees C or less.
[0011] As barrier metal, the multilayer-structure electrode of this invention is an electrode which used either TaSiN or HfSiN, and, specifically, is a multilayer-structure electrode of IrO2/Ir/TaSiN or IrO2/Ir/HfSiN. TaSiN or HfSiN layer which is barrier metal is an about 100-500nm thickness, and can be formed by various technique, such as well-known technique, for example, the RF magnetron spatter method, the DC magnetron spatter method, a vacuum deposition method, and an electron-beam-evaporation method. Here, in order to use TaSiN or HfSiN layer as barrier metal, since amorphous structure is desirable, generally the composition ratio can be changed freely.
[0012] Moreover, Ir layer which constitutes the laminated-structure electrode formed in right above [barrier metal] is IrO [in / it is various technique, such as well-known technique, for example, the RF magnetron spatter method, the DC magnetron spatter method, a vacuum deposition method, and an electron-beam-evaporation method, and / a next process]2. It is desirable to form by sufficient thickness to inhibit oxidization of a lower barrier metal in case of formation of a layer. As for this thickness, 22nm or more is raised. Moreover, as for Ir layer, it is desirable to carry out orientation to a field (111) and to be formed in it. Specifically, in the case of the RF magnetron spatter method, the method of ****ing, using inert gas, such as Ar and N, as spatter gas is raised, holding about [RF power 80-200W] and substrate temperature at about 200-270 degrees C.
[0013] Moreover, IrO2 formed on Ir layer A layer is well-known technique, for example, the same technique as ****, and it is desirable to form by sufficient thickness to inhibit oxidization of a lower barrier metal in case of elevated-temperature annealing of the laminated-structure electrode mentioned later. As for this thickness, 36nm or more is raised. However, it is desirable that the total thickness of IrO2 / Ir layer is formed by 150nm or less and 60 morenm or more. Moreover, IrO2 As for a layer, it is desirable to carry out orientation to a field (100) and to be formed in it. Specifically, in the case of the RF magnetron spatter method, the method of ****ing oxygen gas to inert gas, such as Ar and N, as spatter gas using the gas mixed at about 1:10 to 10:1 rate is raised, holding about [RF power 80-200W] and substrate temperature at about 200-270 degrees C.
[0014] The electrode structure of having sufficient resistance for the heat treatment process in the inside of the oxygen ambient atmosphere 600 degrees C or more is realizable with such a multilayer laminating electrode. Moreover, the laminating electrode structure excellent in the precise surface flat nature which consists of a microcrystal grain is realizable by using the crystal thin film which made the field in IrO2 (100) and made orientation to the field in Ir (111). It is not only suitable as a substratum electrode of a ferroelectric thin film, but the multilayer laminating electrode of the stacking tendency equipped with such surface flat nature and compactness can be controlled also to sheet resistance of the electrode [itself], and it can use it as an electrode of various elements. The multilayer-structure electrode which used the oxide conductor of this invention for below is explained.
[0015] the multilayer-structure electrode of example 1 this invention was shown in drawing 1 -- as -- the front face of the single crystal Si (100) wafer 1 -- SiO2 layer 2 with a thickness of 600nm and a it top -- the barrier metal 3 ****** -- TaSiN (100nm) -- further, on it, as an electrode layer 4, either of IrO2 [IrO2 (230nm), Ir (130nm), and] (82nm)/the Irs (66nm) is formed, and it in addition, composition of TaSiN of this example -- Ta5 SiN4 it was .
[0016] The above-mentioned multilayer-structure electrode is formed as follows. First, it is SiO2 by the oxidizing [thermally] method to Si wafer 1 front face. The layer 2 was formed. Subsequently, this SiO2 TaSiN layer was formed by the spatter on the layer 2. Furthermore, one electrode layer 4 of three kinds of inside was formed by the RF magnetron spatter method on this TaSiN layer. As **** conditions, as RF power 100W, the substrate temperature of 250 degrees C, and 1Pa of gas **s, Ir **** made it as Ar gas, and IrO2 made spatter gas Ar/O2=1 / 1 mixed gas. Moreover, IrO2 / Ir laminated structure continued, after ****ing Ir on condition that the above, and it ****ed and formed IrO2. The morphology on each front face of an electrode had precise and

smooth front-face nature as a result of SEM observation. This is considered to be because for the grain growth in **** to have been suppressed since **** temperature was low temperature comparatively with 250 degrees C.
[0017] Then, in order to investigate the elevated-temperature heat treatment resistance in the inside of oxygen, annealing for 625 degrees C and 10 minutes was given for three kinds of above-mentioned electrodes in the oxygen of the one normal atmosphere. Consequently, sublation of IrO2 accepted with IrO2 / TaSiN structure. It is thought that sublation generated this in order to release the stress in the interface O2 plasma at the time of IrO2 **** and as a result of TaSiN front face's oxidizing by elevated-temperature annealing in the inside of oxygen after that.
[0018] On the other hand, with the Ir/TaSiN structure where O2 plasma is not used at the time of ****, just behind ****, irregularity occurs [the flat electrode front face] after elevated-temperature annealing in the inside of oxygen, and surface flat nature was spoiled. In order to investigate this cause, change of XRD pattern in annealing order was measured. Although it is Ir layer which carried out orientation immediately after **** (111), the oxide IrO2 is generated by annealing. Moreover, it turns out that the peak intensity of Ir (111) reflex is increasing about 40%, and crystallization is also promoted. It is thought as a result of these oxidization and crystallization (grain growth) that the irregularity of Ir electrode front face occurred.
[0019] The above result, in order for sublation of a layer or the irregularity on the front face of an electrode to all occur by the oxidation reaction by elevated-temperature annealing processing in oxygen after the time of layer formation, or formation etc. and to form an oxide ferroelectric thin film with IrO2 / TaSiN structure, and Ir/TaSiN structure, as a lower electrode, it is unsuitable. Next, if it sees about IrO2/Ir/TaSiN structure, as shown in drawing 2 , after elevated-temperature annealing in oxygen does not accept, but occurrence of sublation, a hillock, etc. serves as the precise layer with which the flat nature on the front face of an electrode was also further maintained at the EQC the annealing front. Moreover, it is before and after annealing also from XRD measurement, and change of a diffraction pattern is not seen, but it turns out that the orientation membrane structure of IrO2 (100)/Ir (111) is obtained.
[0020] These results are forming Ir layer on TaSiN, and it is not necessary to expose a direct TaSiN front face to an oxygen plasma on it at the time of IrO two-layer ****, Furthermore Ir front face oxidizes slightly, the oxidizing zone IrO2 suppresses oxidization of TiSiN interface, and since **** temperature is as low as 250 degrees C, the flat nature on the front face of Ir is not spoiled, It is thought that it was obtained when the IrO two-layer formed in the top had suppressed oxidization of the lower part by the oxygen diffusion at the time of annealing of Ir/TaSiN.
[0021] When sheet resistance with this IrO2/Ir/TaSiN structure was measured, just behind ****, about 1.2ohms / ** is obtained and a significant change did not have after annealing. Sheet resistance with Pt(100nm)/TiN / Ti structure where of it is used conventionally is about 1ohm/**, and it was checked from sheet resistance almost of the same grade being obtained that it can fully be used as an electrode.
[0022] Moreover, a precise electrode can be produced by the surface flatness which has neither sublation nor a hillock similarly in the IrO2/Ir/HfSiN structure where HfSiN was used for barrier metal, and it was checked that there is elevated-temperature annealing resistance in the inside of oxygen.
[0023] It is the structure where the substructure was chosen from any one, TaSiN and the HfSiN, in the electrode structure which was described above and which is formed on a semiconductor substrate like, and the multilayer electrode which has IrO2 / Ir laminated structure which becomes the upper part from IrO2 of crystalline orientation (100) and Ir of orientation (111) has the annealing process resistance in the inside of the oxygen ambient atmosphere 600 degrees C or more. That is, becoming the electrode which has the above-mentioned process resistance was shown by by having a thickness more than the thickness which has a thickness more than the thickness in which Ir layer inhibits oxidization of TaSiN which is a substructure in case of IrO two-layer formation, and HfSiN, and inhibits oxidization of the barrier metal TaSiN and HfSiN whose IrO two-layer is a substructure by the elevated-temperature annealing process in the inside of oxygen. Moreover, this electrode is equipped with surface flat nature and compactness, and has the outstanding electrical property of the same grade as it of Pt/TiN / Ti structure also for sheet resistance.
[0024] Example 2 substrate and **** conditions produced the sample of the IrO2/Ir/TaSiN structure where each thicknesss differ, using the same thing as an example 1. However, the thickness of 36-82nm and Ir layer of orientation (111) was produced for the IrO two-layer thickness of orientation (100) in 15-66nm. Here, the thickness was controlled by changing spatter **** time. About the electrode structure where thicknesss differ respectively, the same annealing as an example 1 was performed.
[0025] With the IrO2 (82nm) / Ir(15nm)/TaSiN structure where the thickness of Ir layer is as thin as 15nm, the hillock was observed after annealing. It is thought as IrO2 exfoliated with IrO2 / TaSiN structure shown in the example 1 that this is the same cause. That is, since the thickness of Ir layer is very thin, since a thickness is thin, the part where TaSiN oxidizes exists in the grade which can be finishing wearing TaSiN front face completely, or cannot inhibit oxidization by the oxygen plasma at the time of subsequent IrO2 formation, and it is thought that the stress of a there generated the hillock.
[0026] About other samples, sublation, a hillock, etc. are not altogether seen after annealing, but it has checked that there was annealing resistance. When SEM observation of the cross section after annealing of the IrO2 (36nm) / Ir(22nm)/TaSiN structure where a thickness is the thinnest was carried out in the produced sample, when the thickness of IrO2/Ir is as thin as about 60nm, flat nature is maintained, and, as for the reaction, the diffusion, etc., TaSiN fraction was not seen, either.
[0027] That is, by using IrO2 / Ir laminating electrode structure which consists of IrO2 which carried out orientation to (100), and (111) Ir which carried out orientation, it was very precise and the about 60nm thin thin film has realized **** process resistance of an oxide ferroelectric thin film. Furthermore, when sheet resistance was measured about the produced sample, it turns out that sheet resistance of the whole electrode is controllable by changing a thickness Ir layer in IrO2 / Ir laminating electrode, and IrO

two-layer as shown in drawing 3 in the domain of 1.2-2.8ohms / **.
[0028] Moreover, also in the IrO2/Ir/HfSiN structure using HfSiN as barrier metal, it has checked that could produce the flat and precise electrode structure which does not have sublation and a hillock similarly in the domain whose thickness of IrO2 / Ir electrode is about 60nm - 150nm at least, and the elevated-temperature annealing resistance in the inside of oxygen was acquired. As stated above, the electrode which was excellent in using IrO2 / Ir electrode structure of this invention at flat nature and compactness is producible. Consequently, the electrode the thickness of Ir layer is 22nm or more, and the IrO two-layer thickness excelled [electrode] in the process resistance with the as thin thickness of IrO2 / Ir electrode as about 60-150nm in conditions 36nm or more was producible. Furthermore, when sheet resistance changed the thickness of each class, it was controllable to 1.1-2.8ohm/**.
[0029]
[Effect of the invention] According to this invention, the lower electrode excellent in process resistance indispensable to utilization of the ferroelectric memory and DRAM using STC structure can create with sufficient repeatability. Especially, IrO two-layer and Ir layer are crystal thin films, and in carrying out orientation of the IrO two-layer to a field (100) and coming to carry out orientation of the Ir layer to a field (111), since the electrode is excellent also in flat nature and compactness, applicability, such as a micro-processing process, also becomes high.
[0030] Furthermore, when the thickness of IrO2 / Ir layer is 150nm or less, a control of electrical properties, such as sheet resistance, also becomes possible by changing the thickness of each class of a laminated-structure electrode. Thus, in the multilayer-structure electrode of this invention, for example in the formation process of a ferroelectric layer, the reaction with a lower semiconductor and counter diffusion can be prevented, and it is enabled to obtain the element which has a reliable good property.

[Translation done.]